

FIG.1

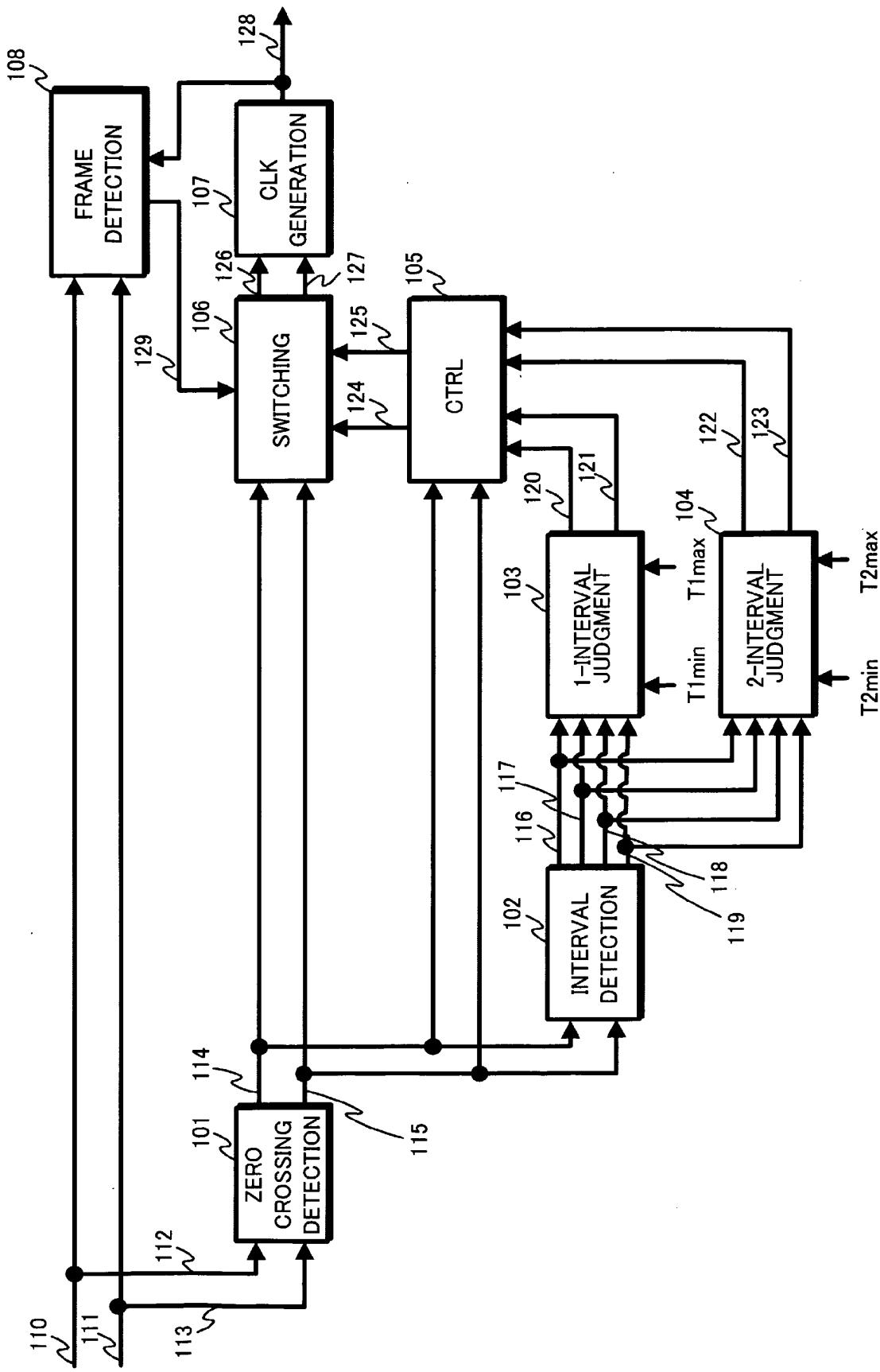


FIG. 2

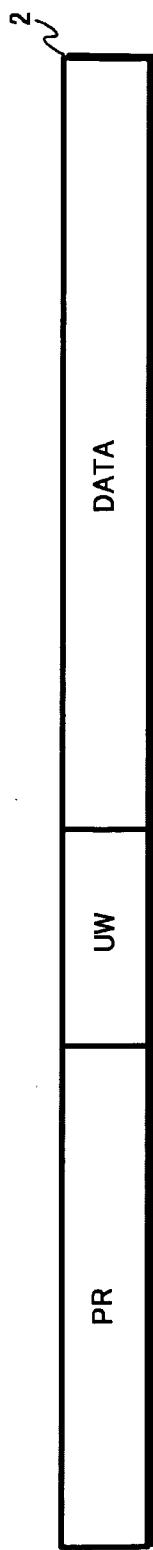


FIG. 3

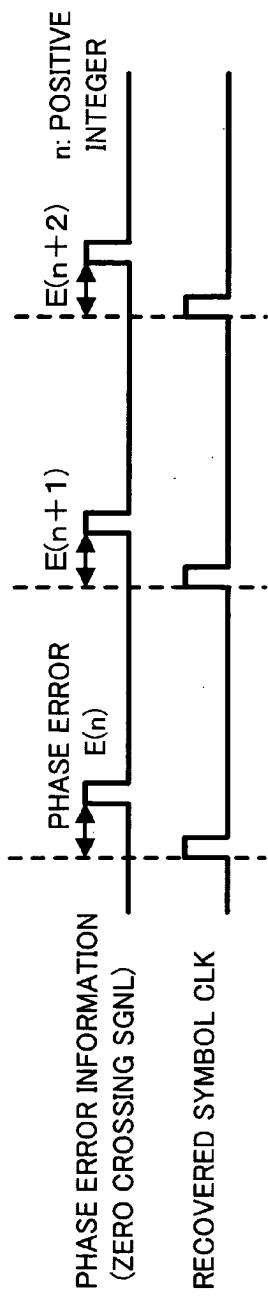


FIG. 4

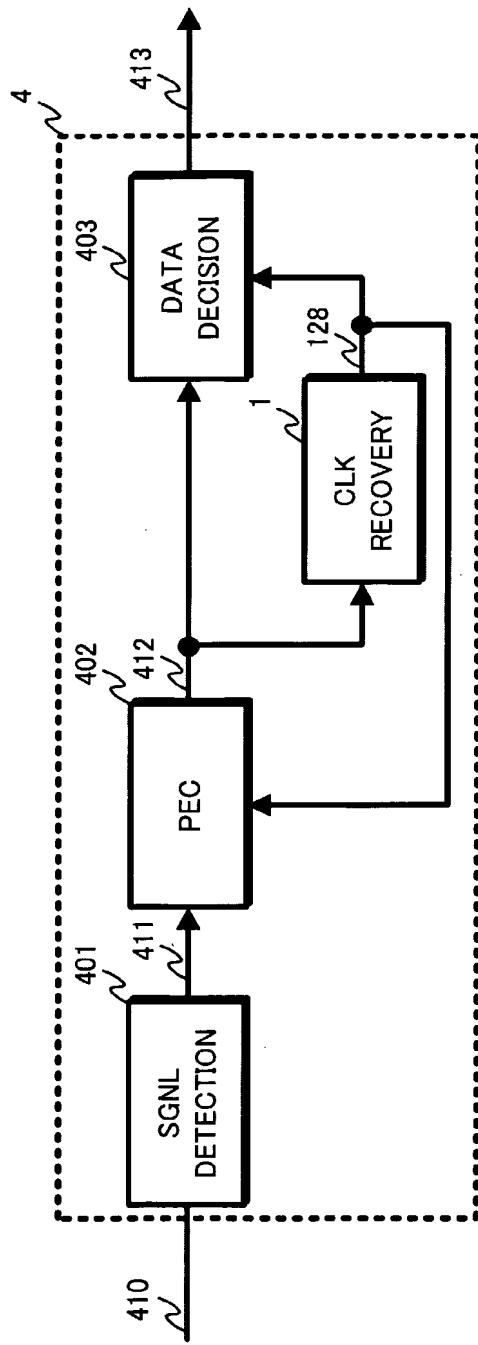


FIG. 5

BIT $X_n \ X_{n+1}$	PHASE TRANSITION
1 1	$-3\pi/4$
0 1	$3\pi/4$
0 0	$\pi/4$
1 0	$-\pi/4$

FIG. 6

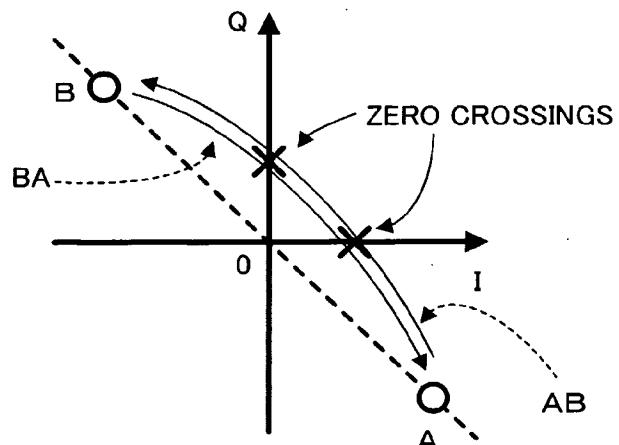


FIG. 7

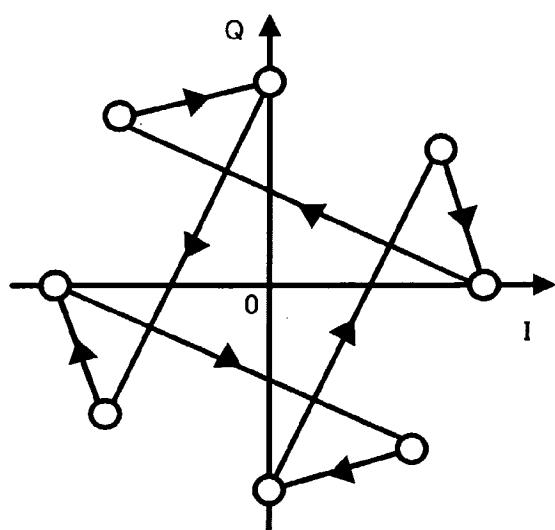


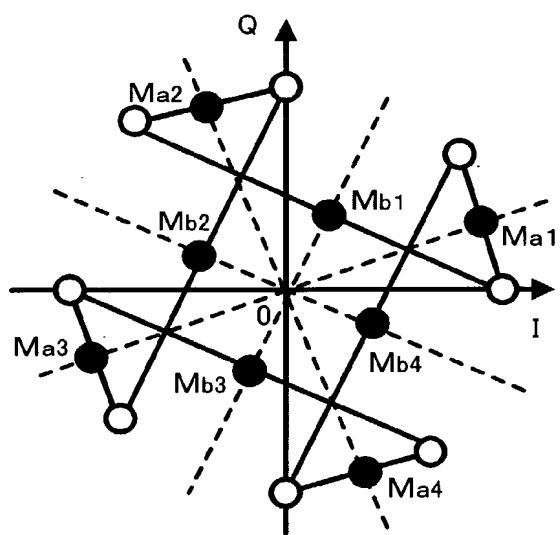
FIG. 8

FIG. 9

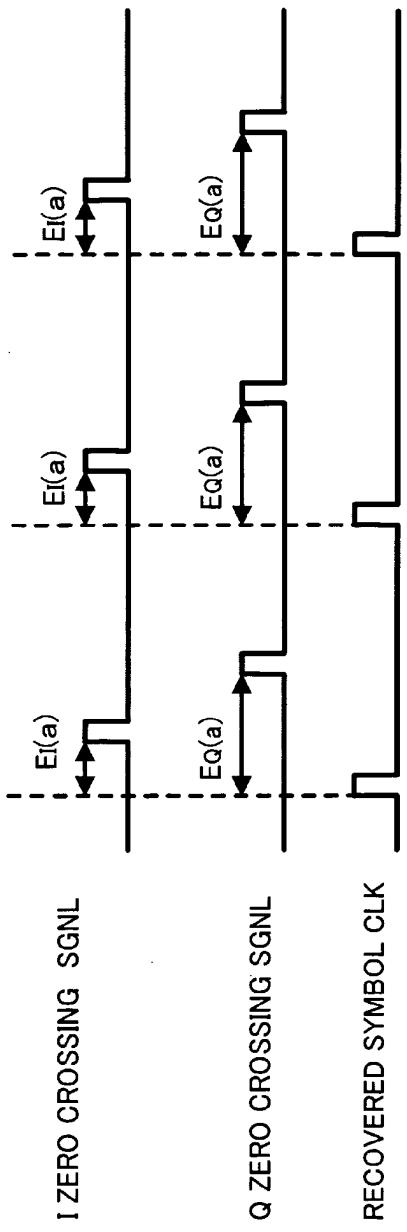


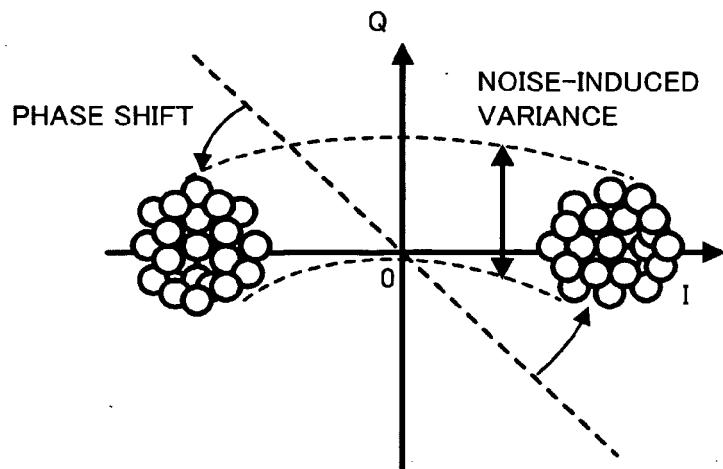
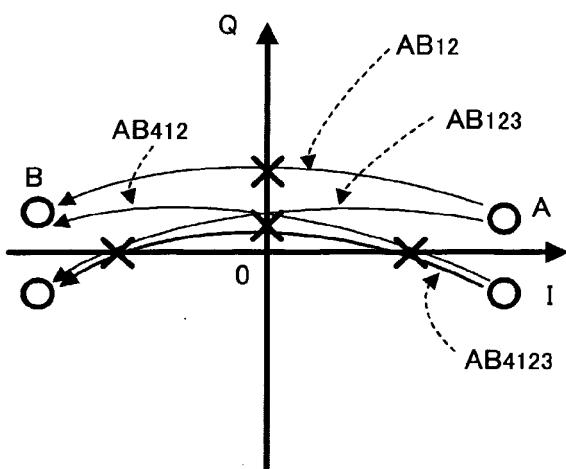
FIG. 10**FIG. 11**

FIG.12

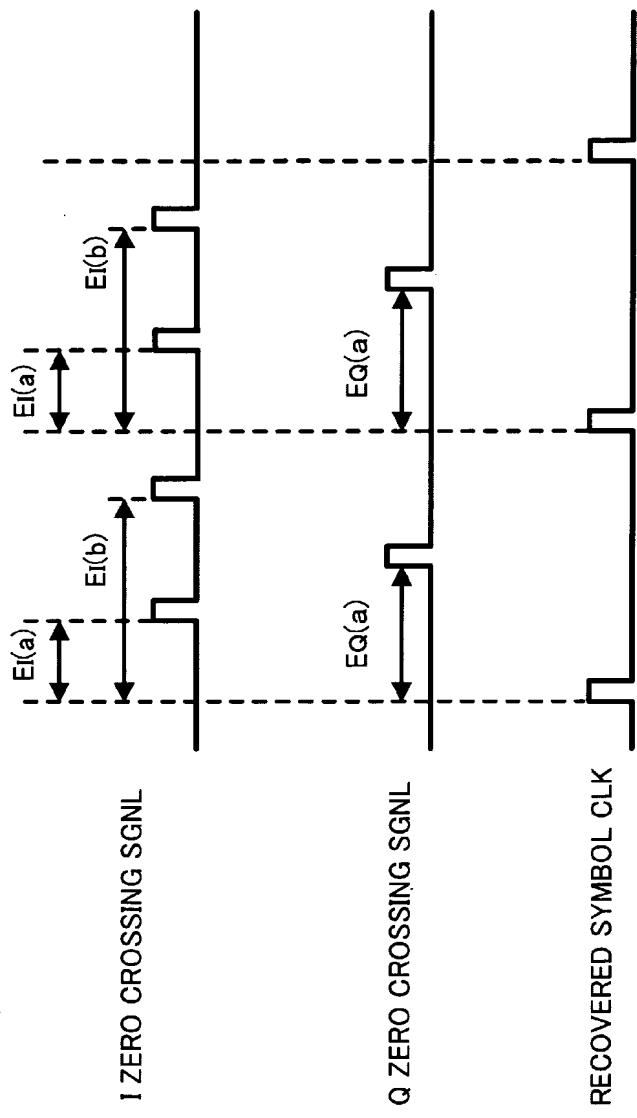


FIG.13

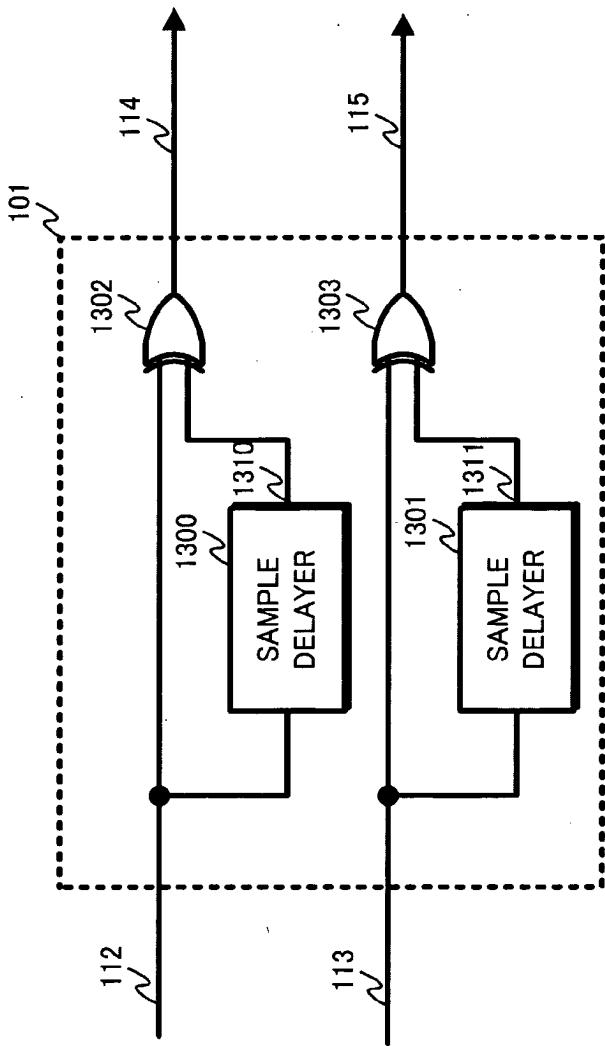


FIG.14.

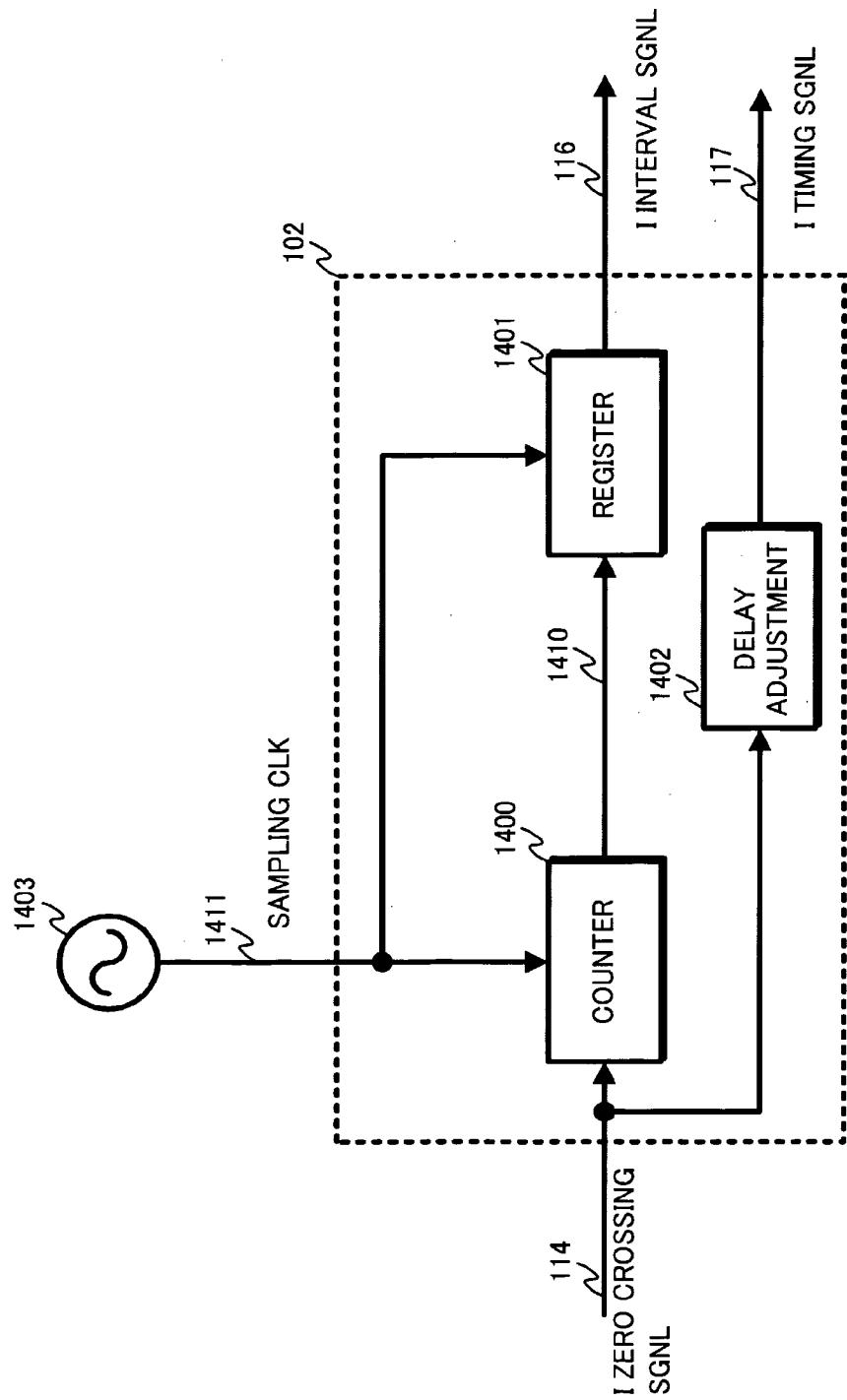


FIG.15

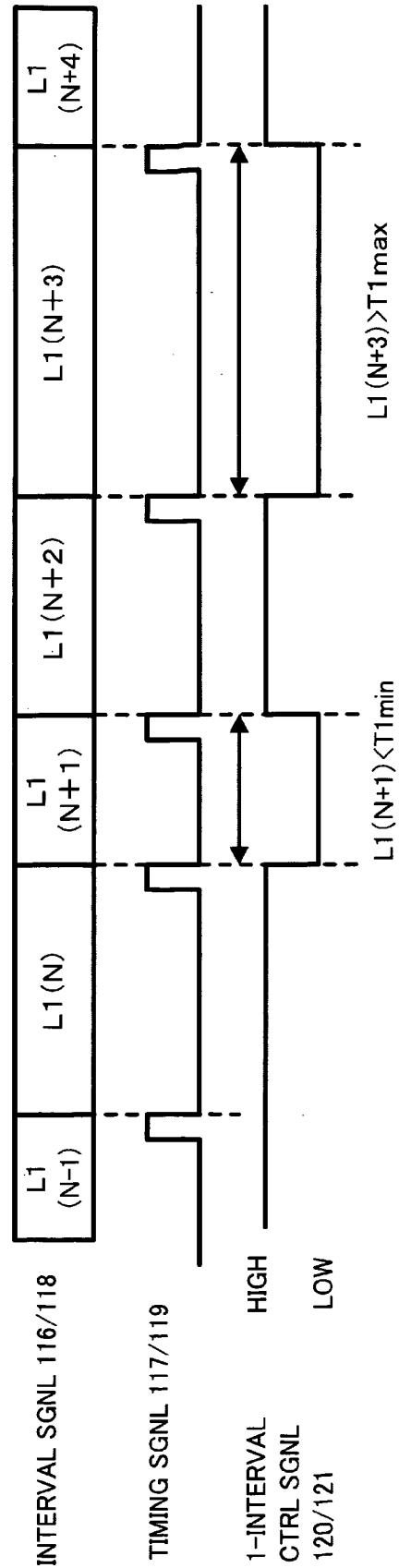


FIG. 16

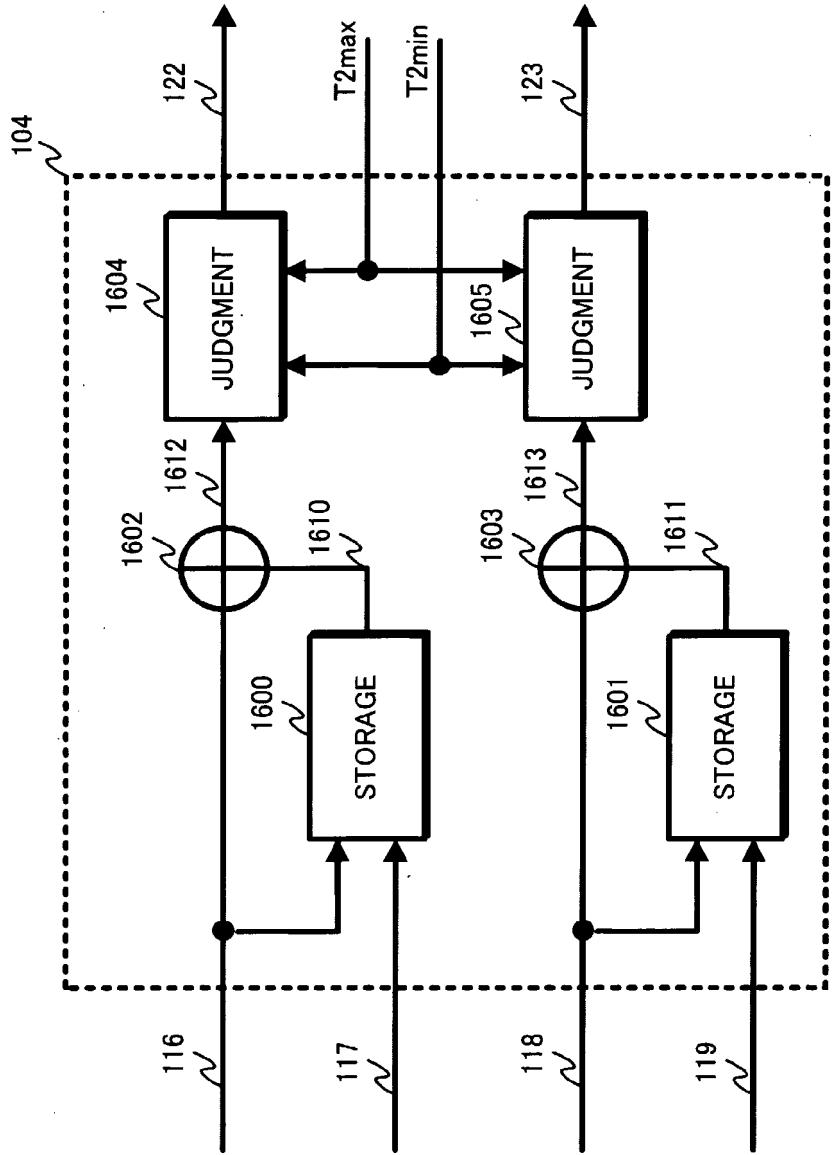


FIG.17

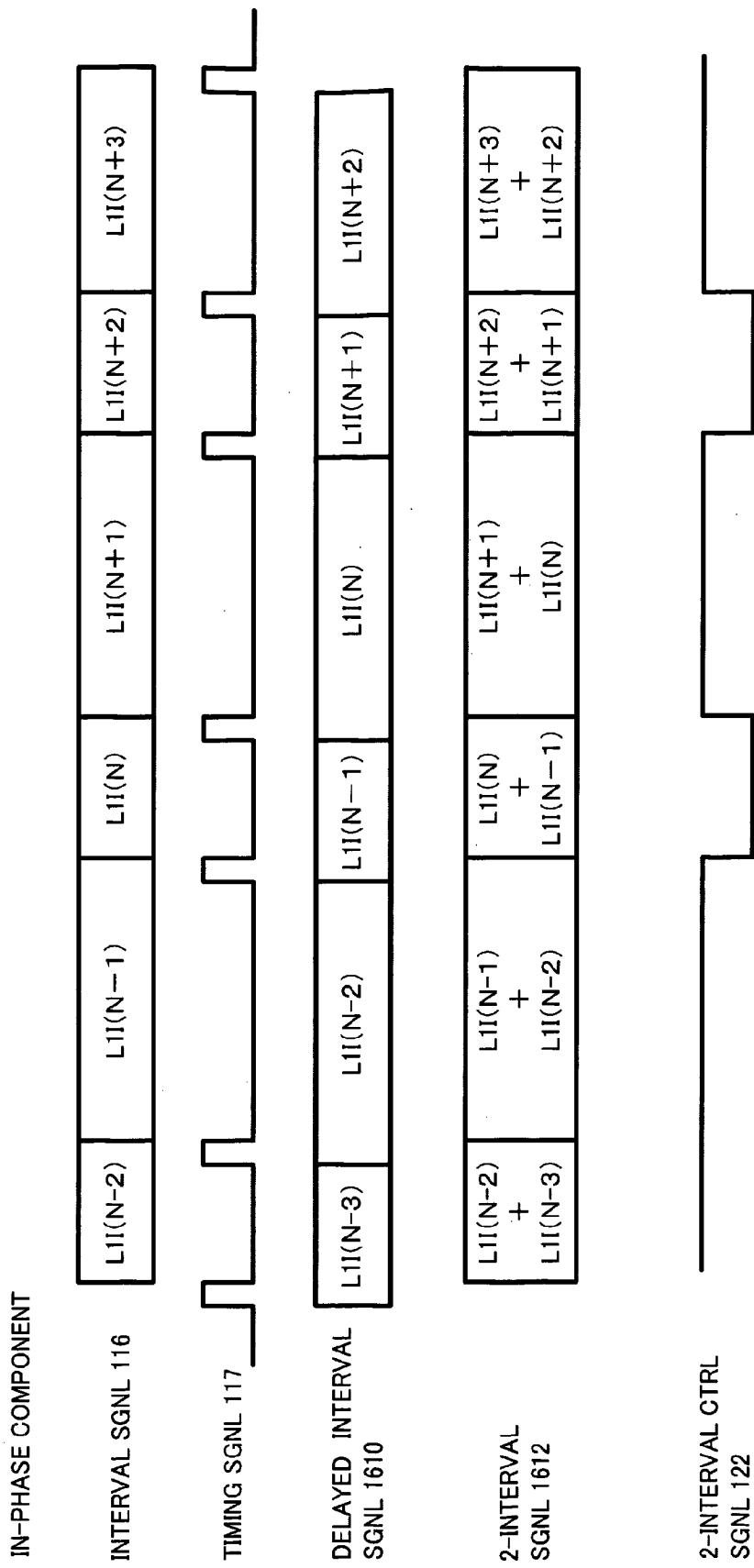


FIG.18

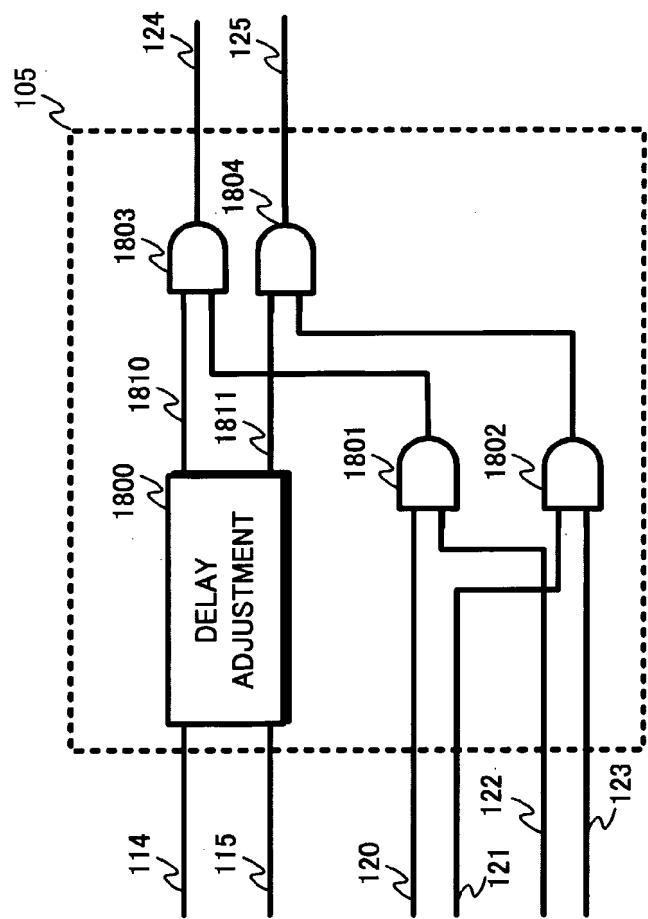


FIG.19

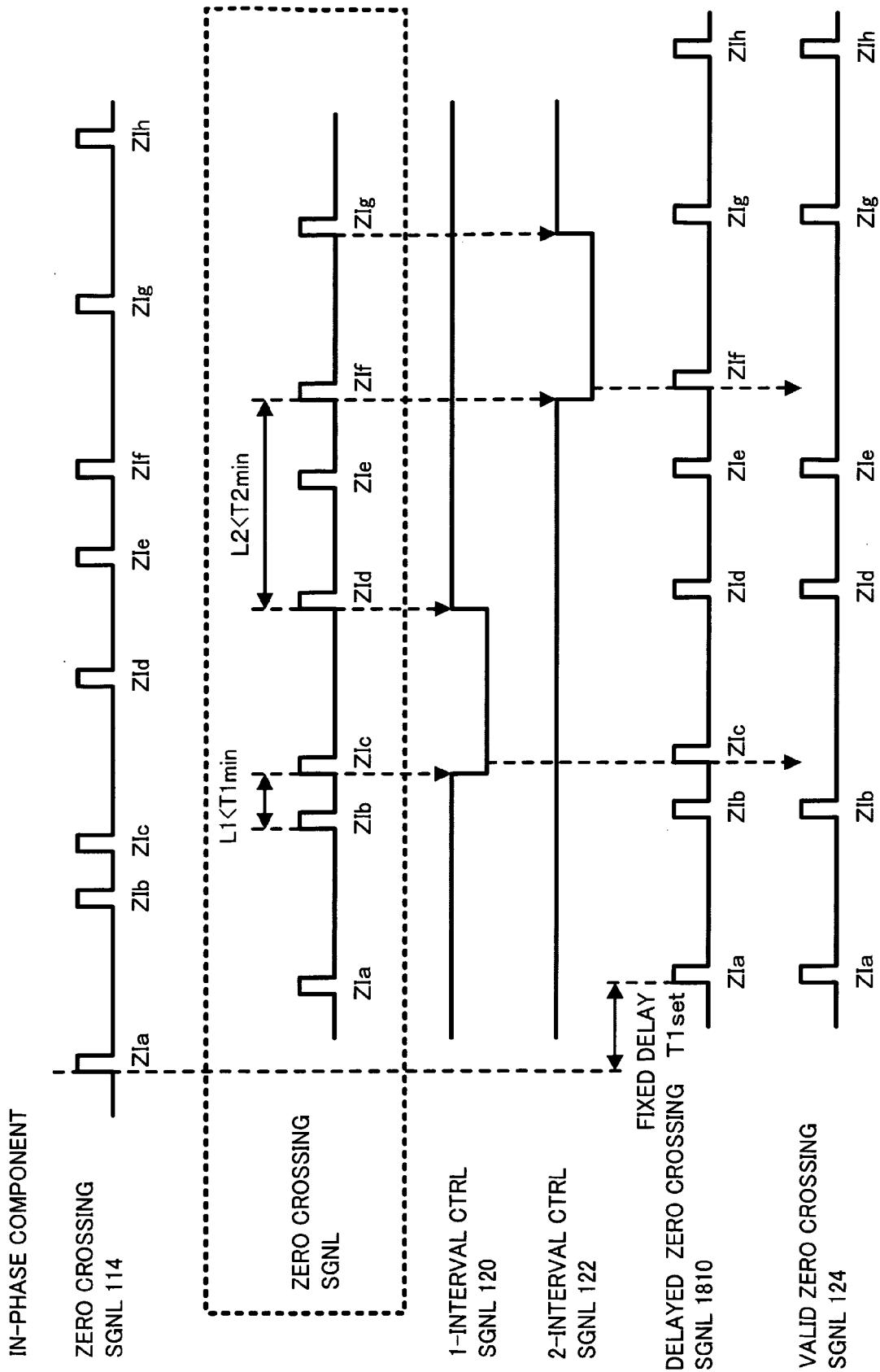


FIG.20A

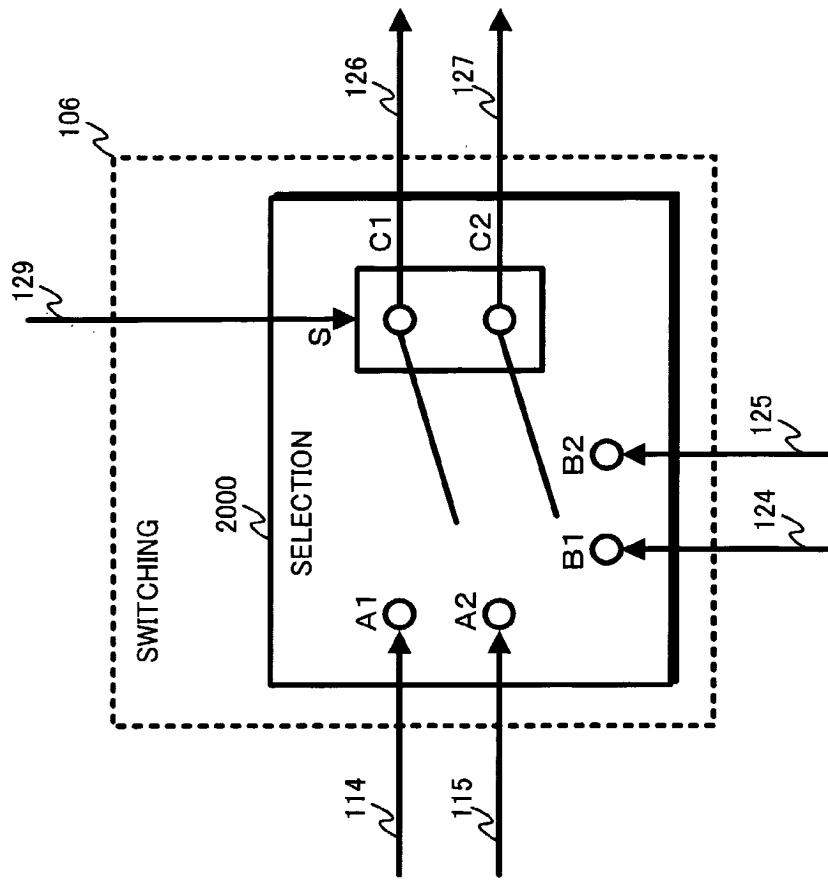


FIG.20B

TRUTH TABLE	
CONTROL SIGNAL S	OUTPUT (C_1, C_2)
0	(B_1, B_2)
1	(A_1, A_2)

FIG.21

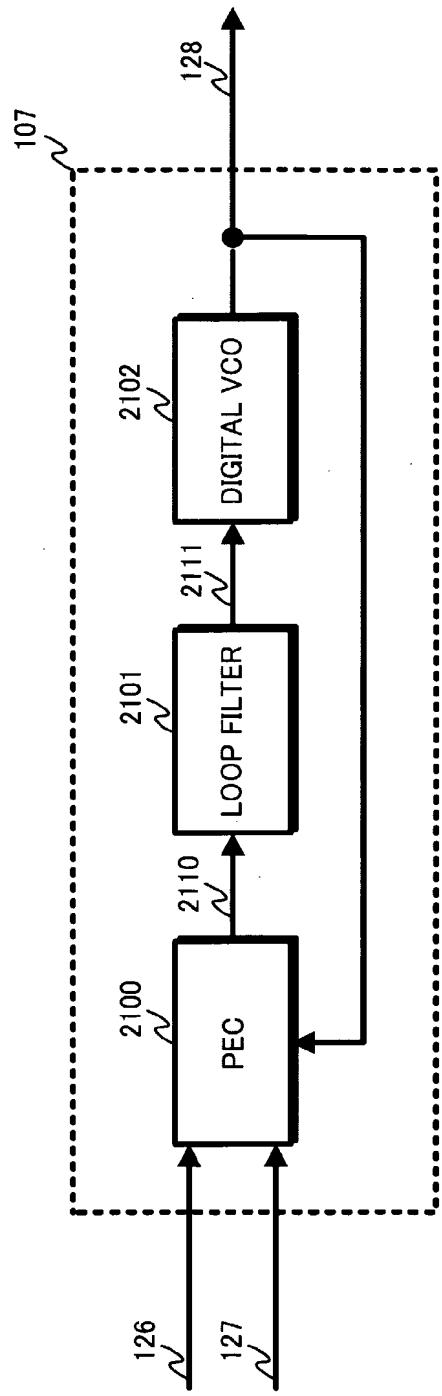


FIG.22

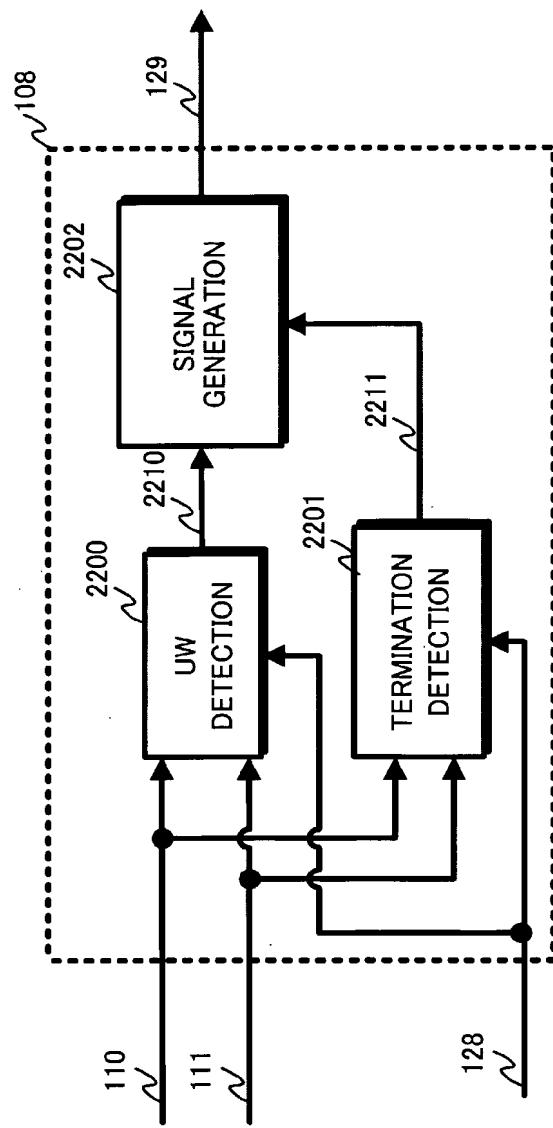


FIG.23

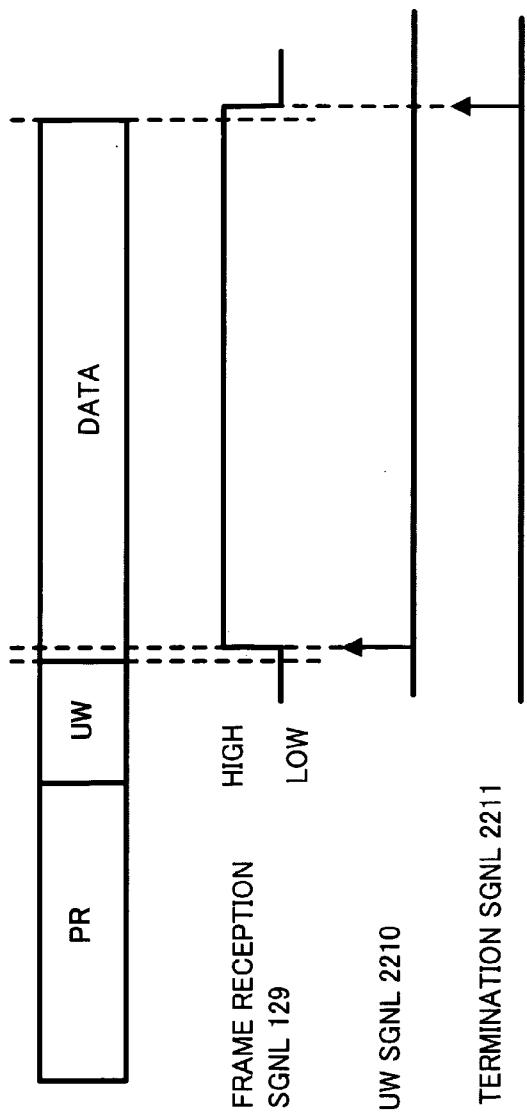
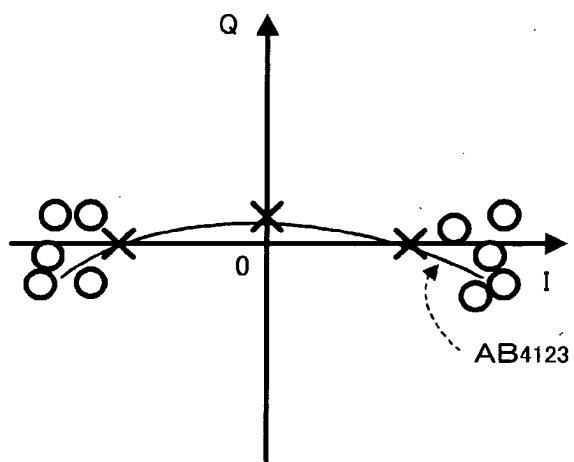


FIG.24



IN-PHASE COMPONENT

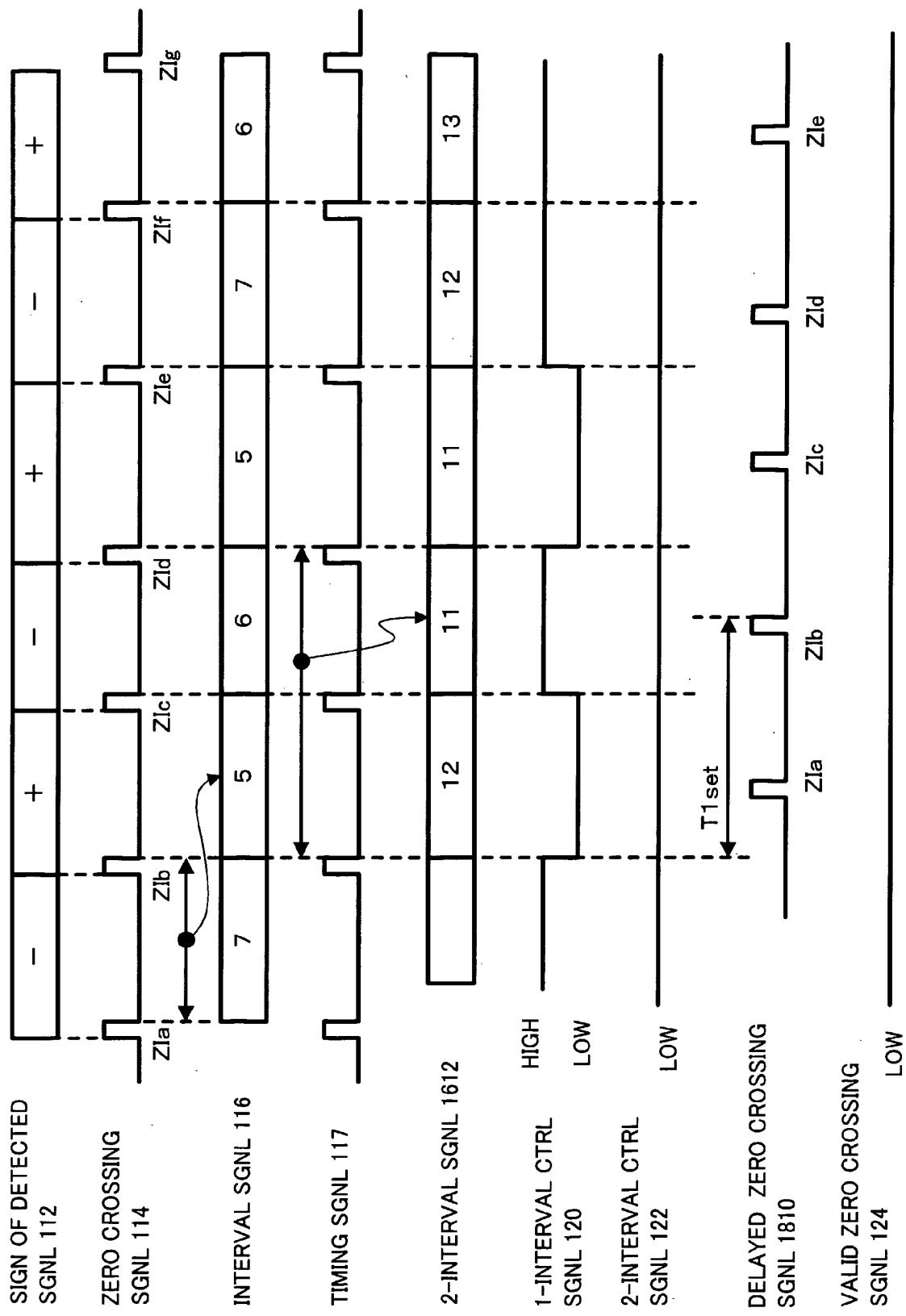


FIG.25

QUADRATURE COMPONENT

SIGN OF DETECTED
SGNL 113

ZERO CROSSING
SGNL 115

INTERVAL SGNL 118

TIMING SGNL 119

2-INTERVAL
SGNL 1613

1-INTERVAL
CTRL SGNL 121

2-INTERVAL
CTRL SGNL 123

DELAYED ZERO CROSSING
SGNL 1811

VALID ZERO CROSSING
SGNL 125

FIG.26

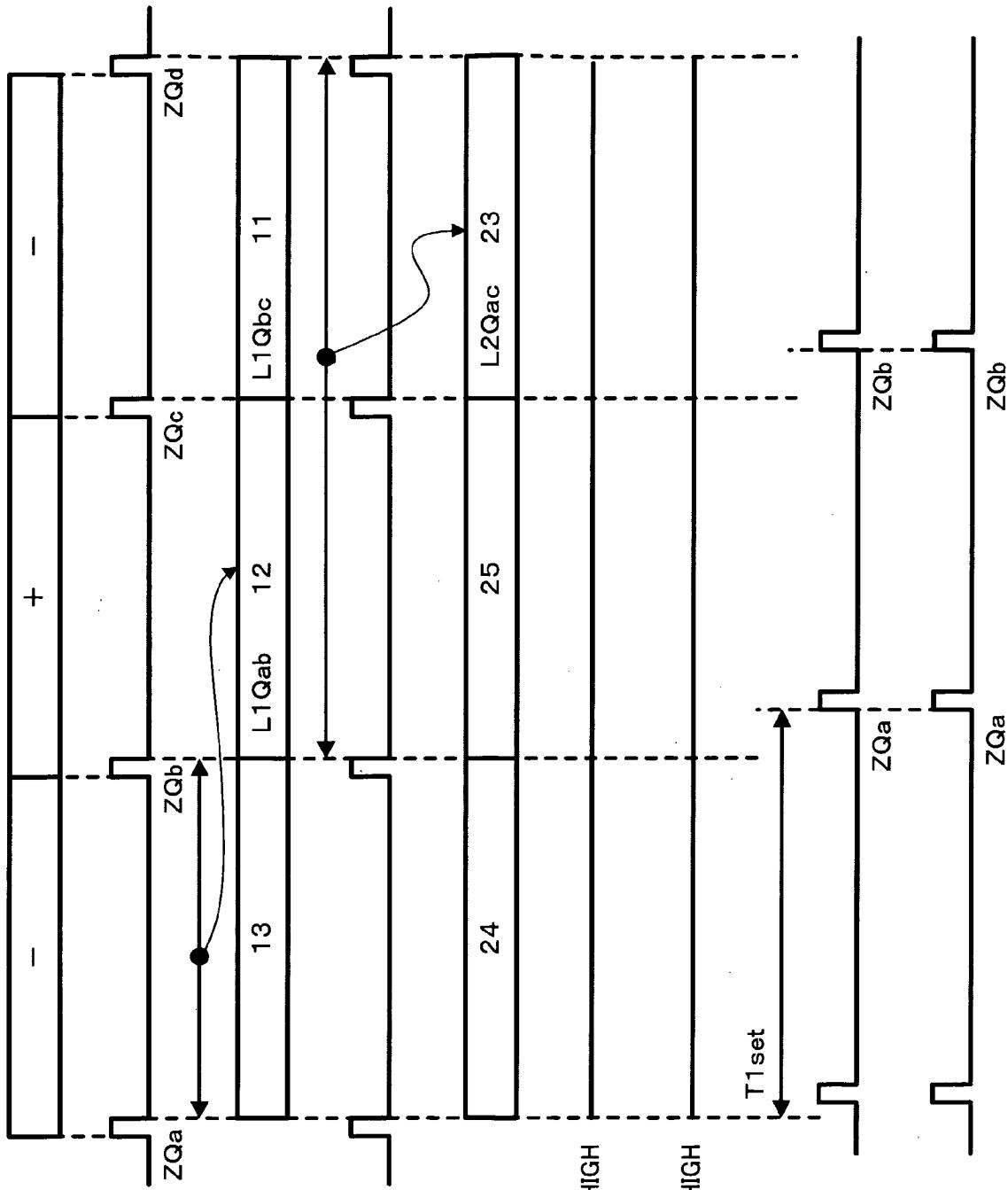


FIG.27

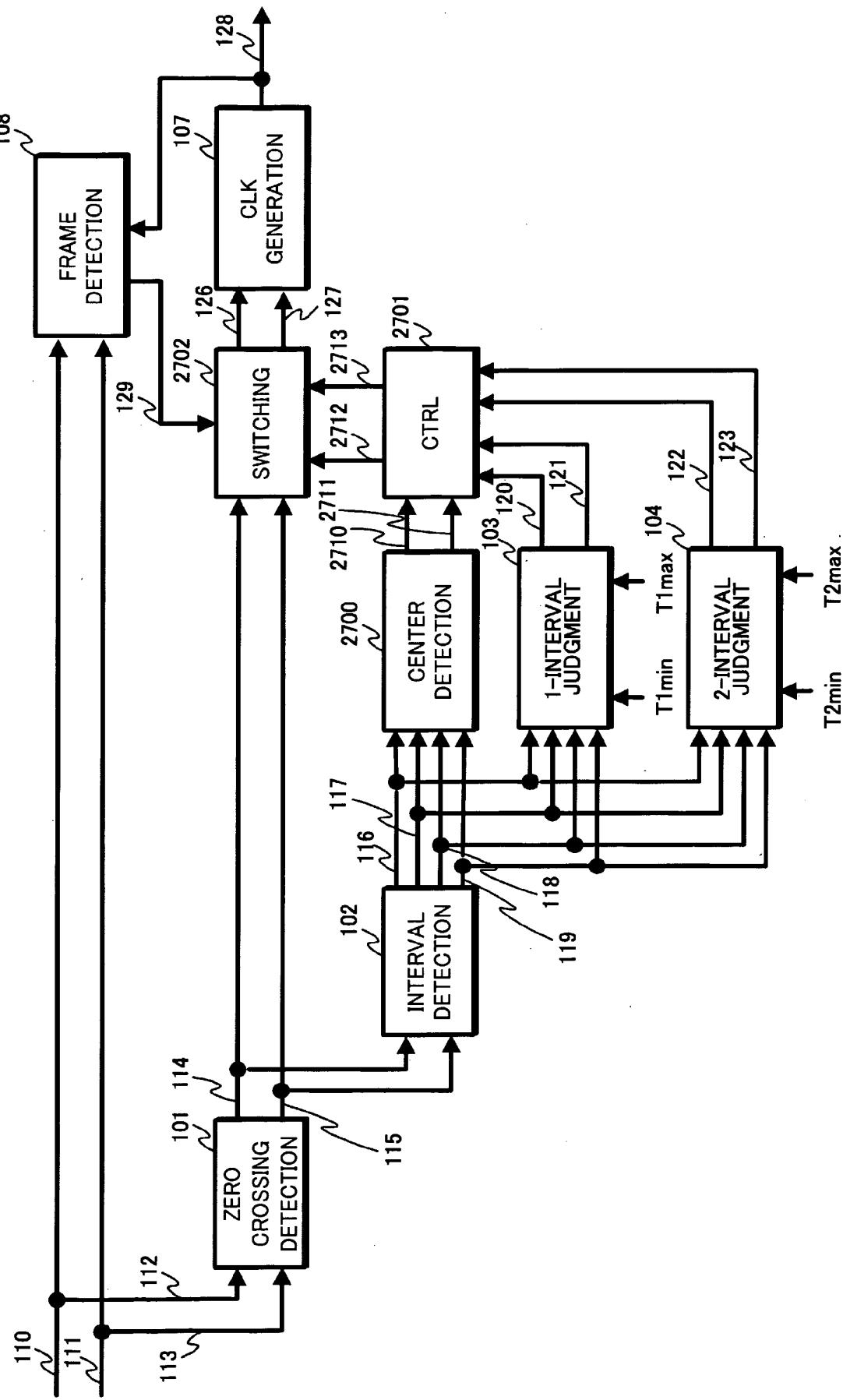


FIG.28

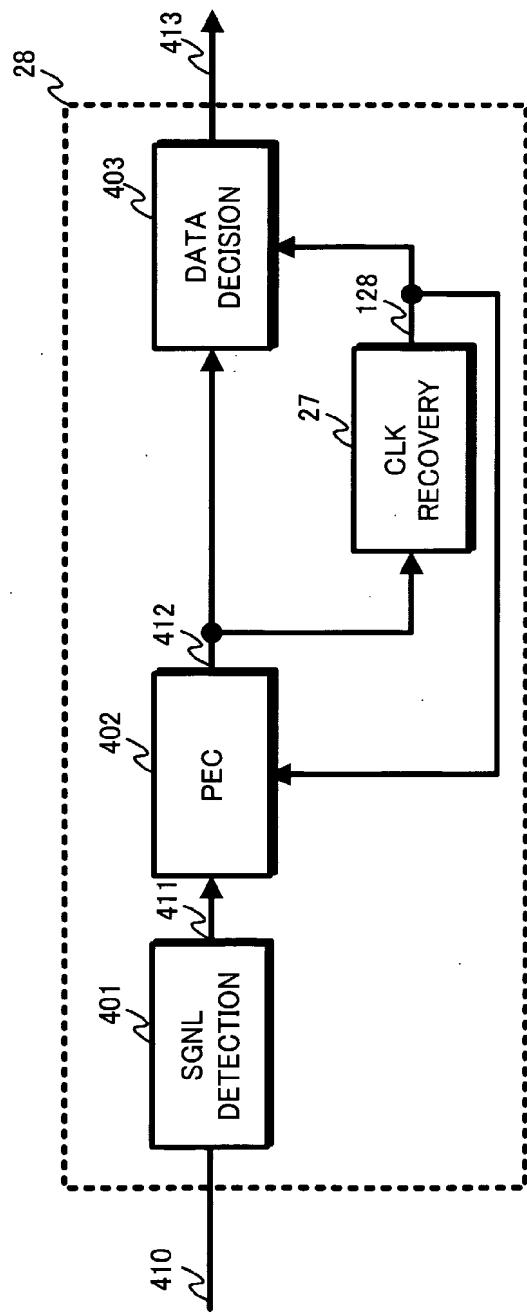


FIG.29

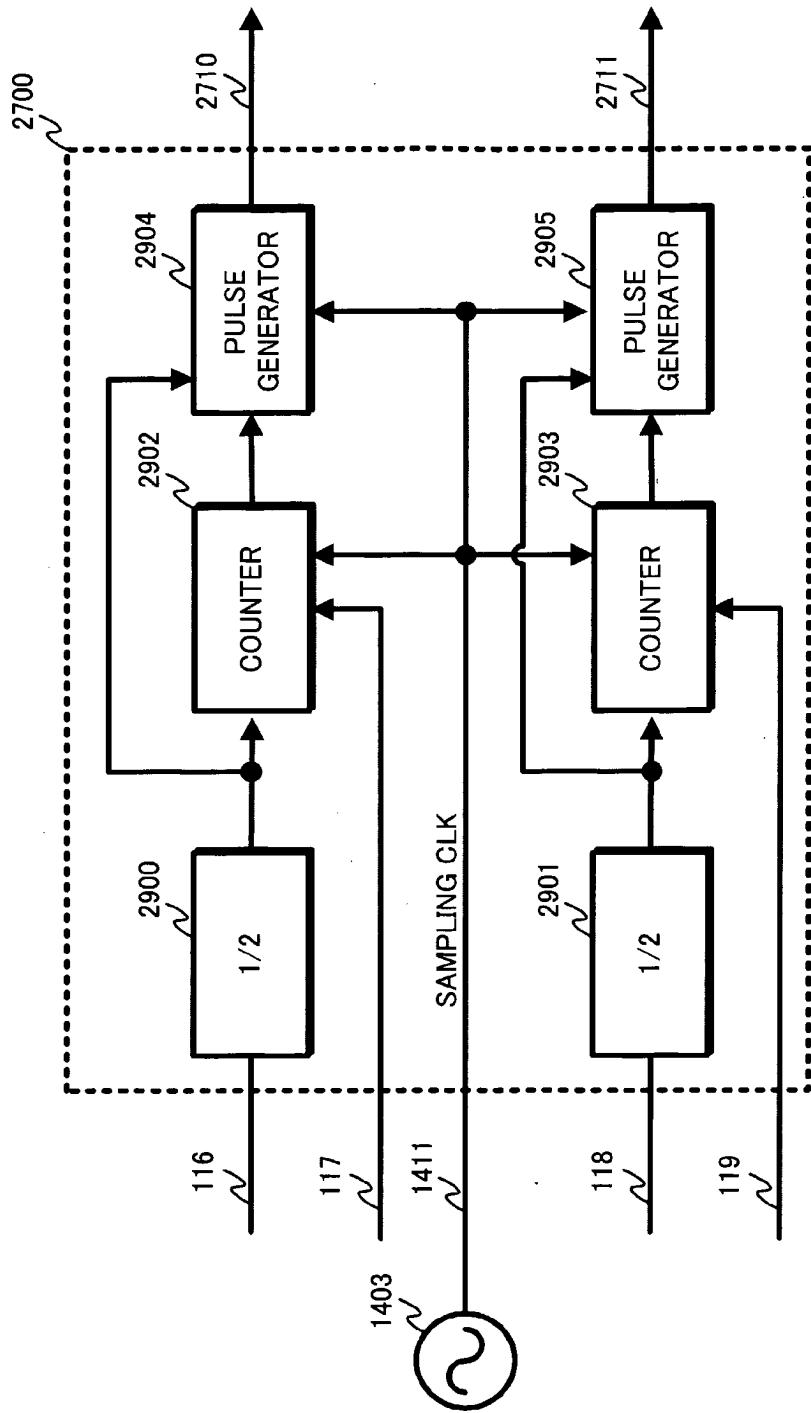


FIG.30

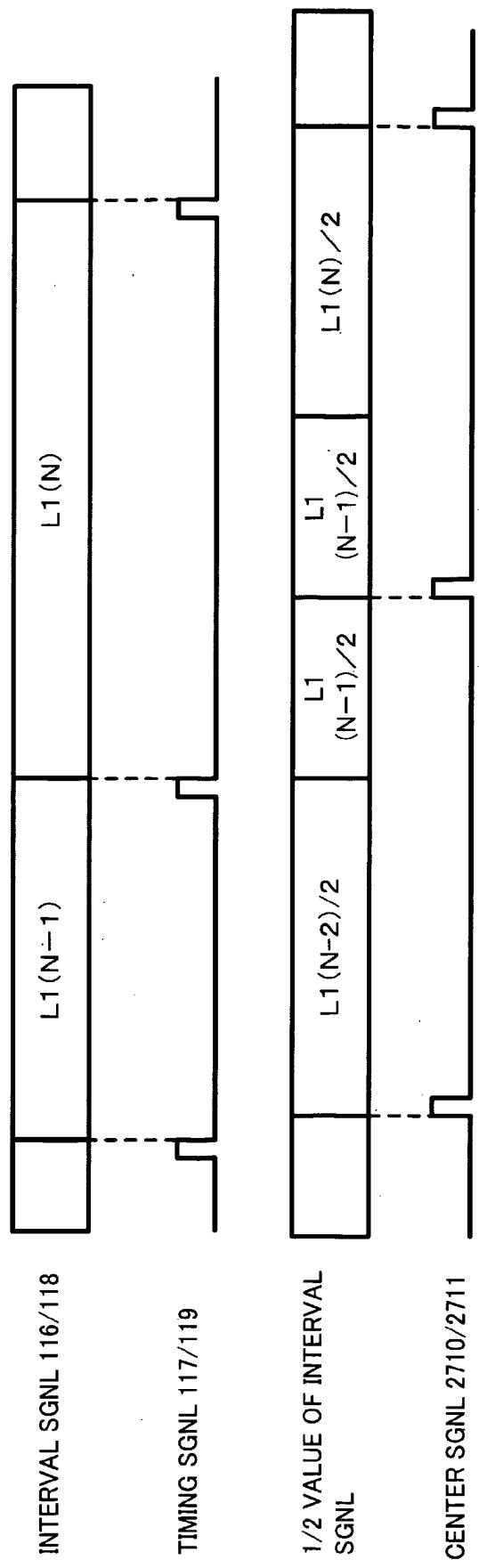


FIG.31

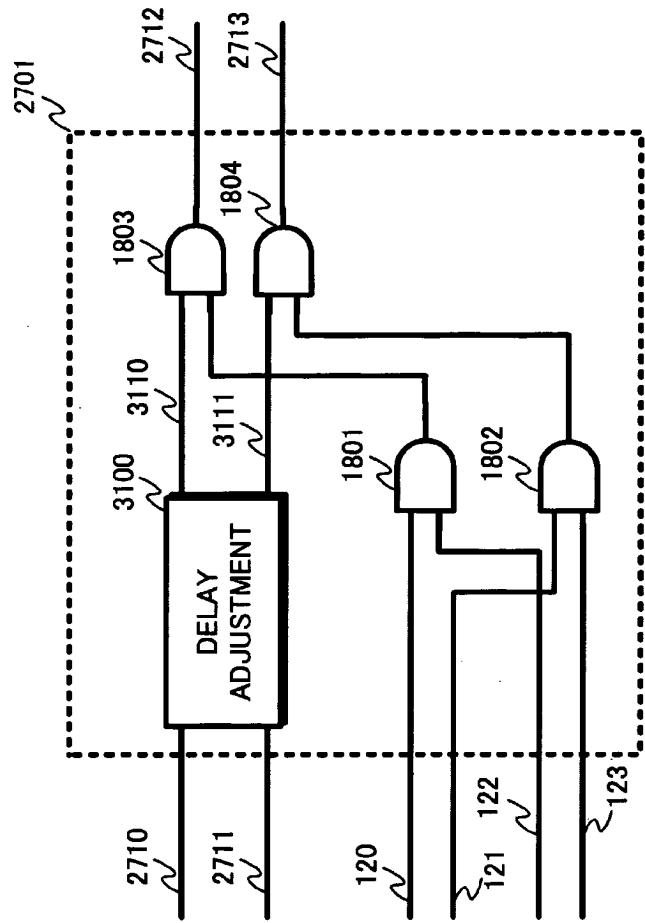


FIG.32

IN-PHASE COMPONENT

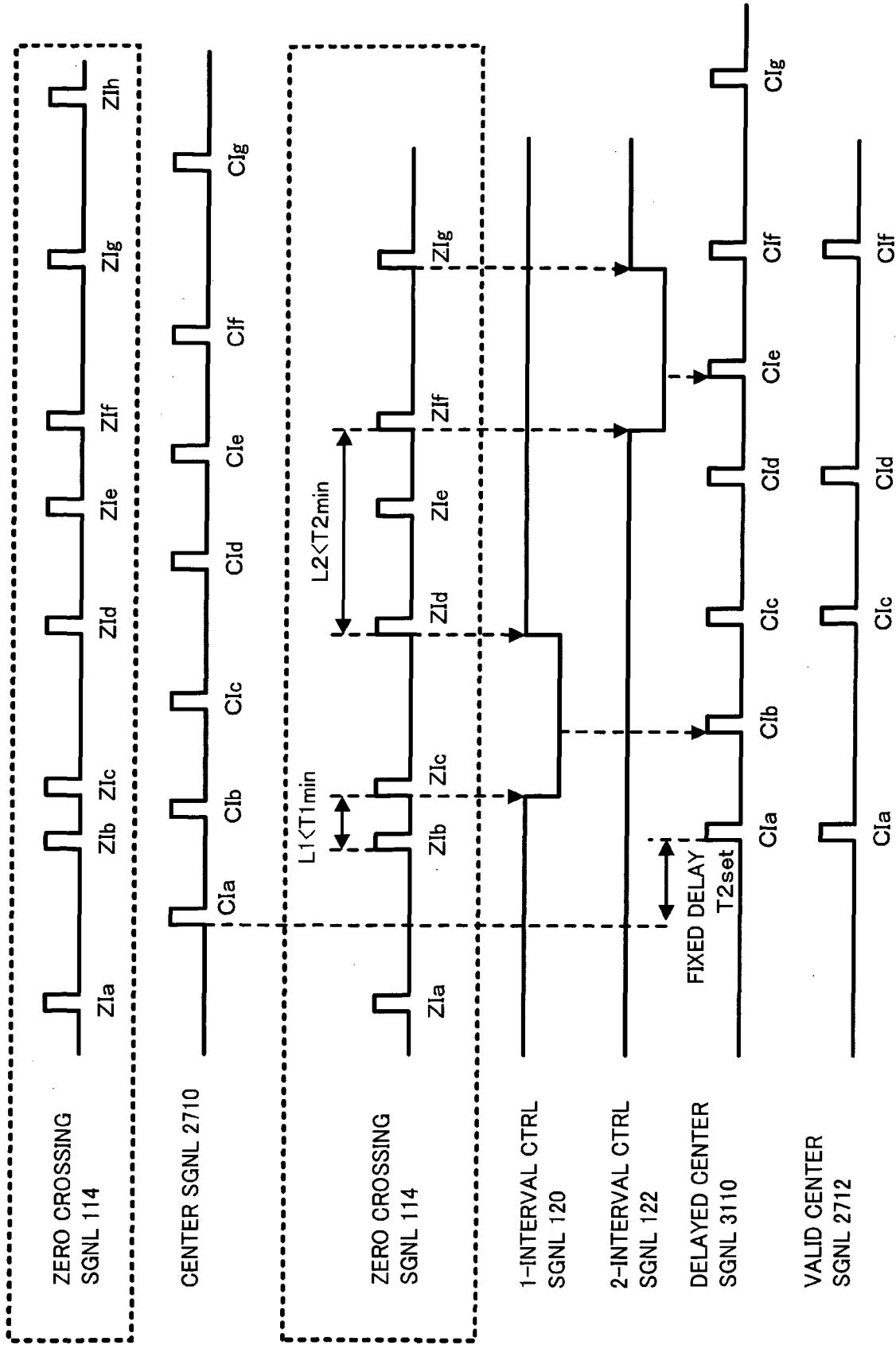


FIG.33

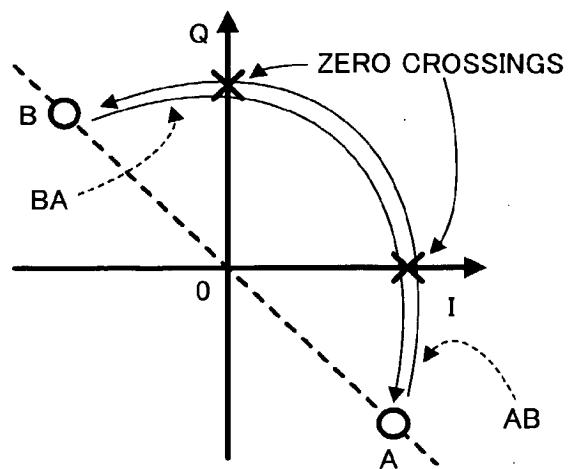


FIG.34

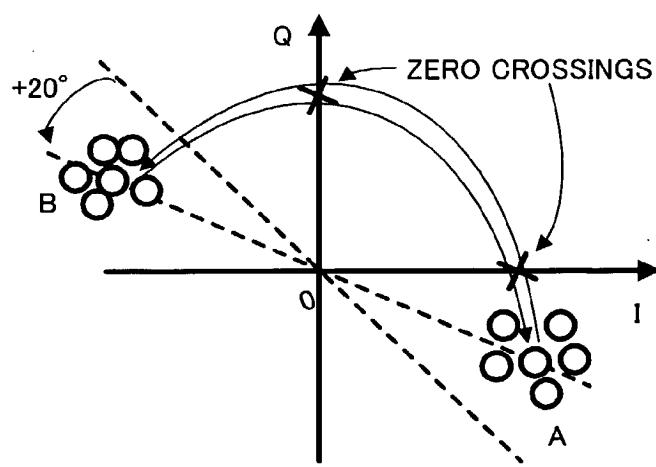
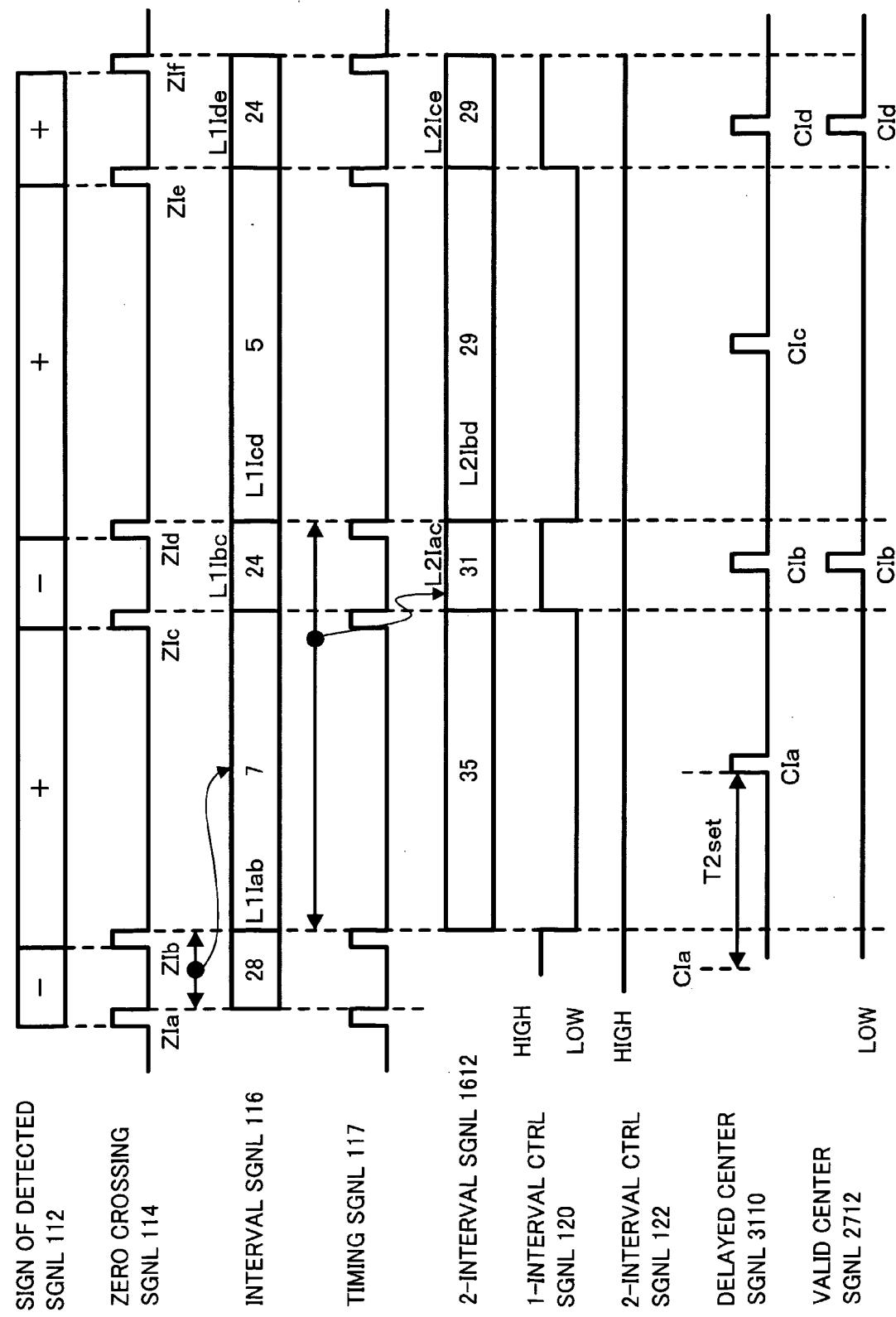


FIG.35

IN-PHASE COMPONENT



QUADRATURE COMPONENT

FIG.36

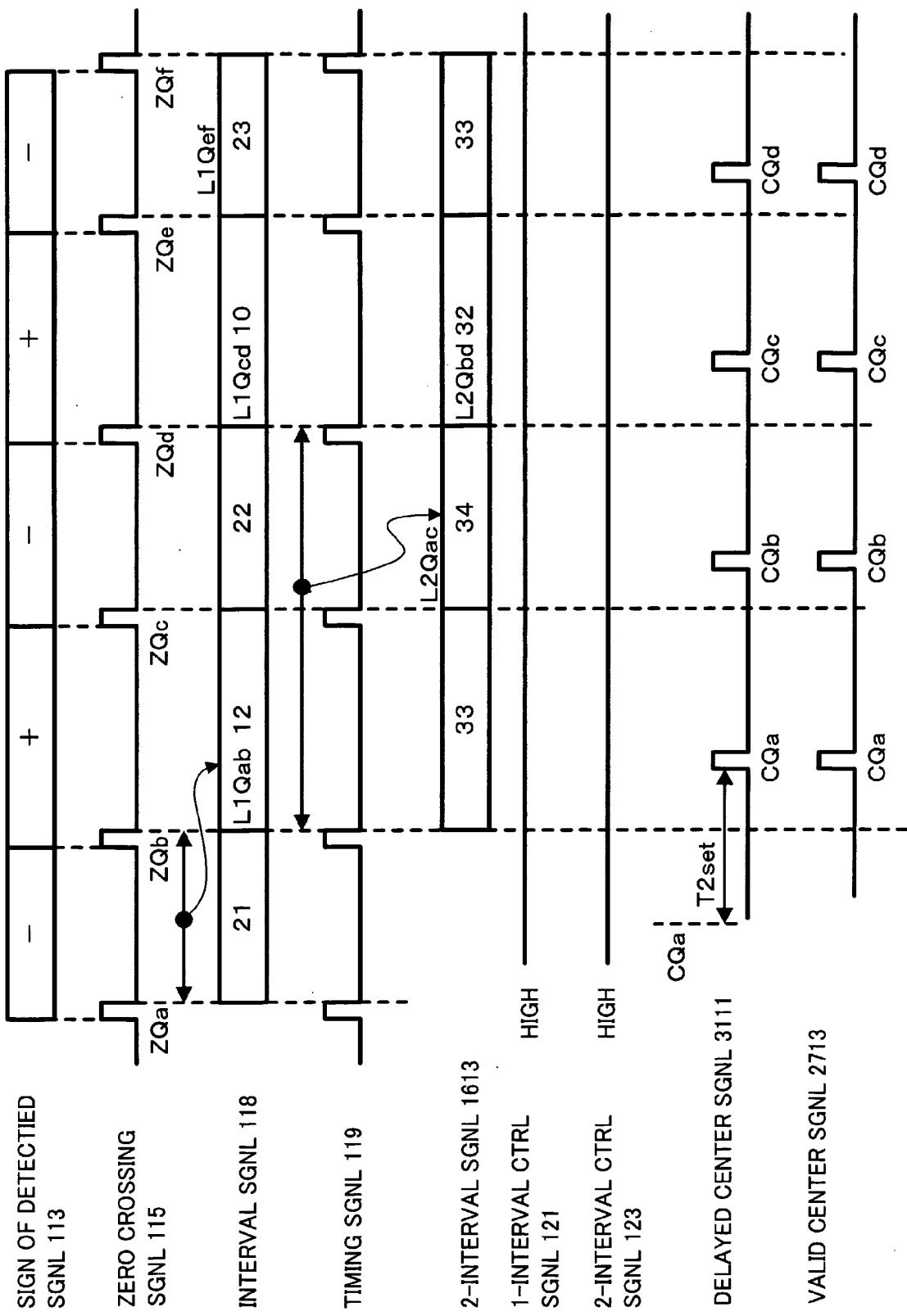


FIG.37

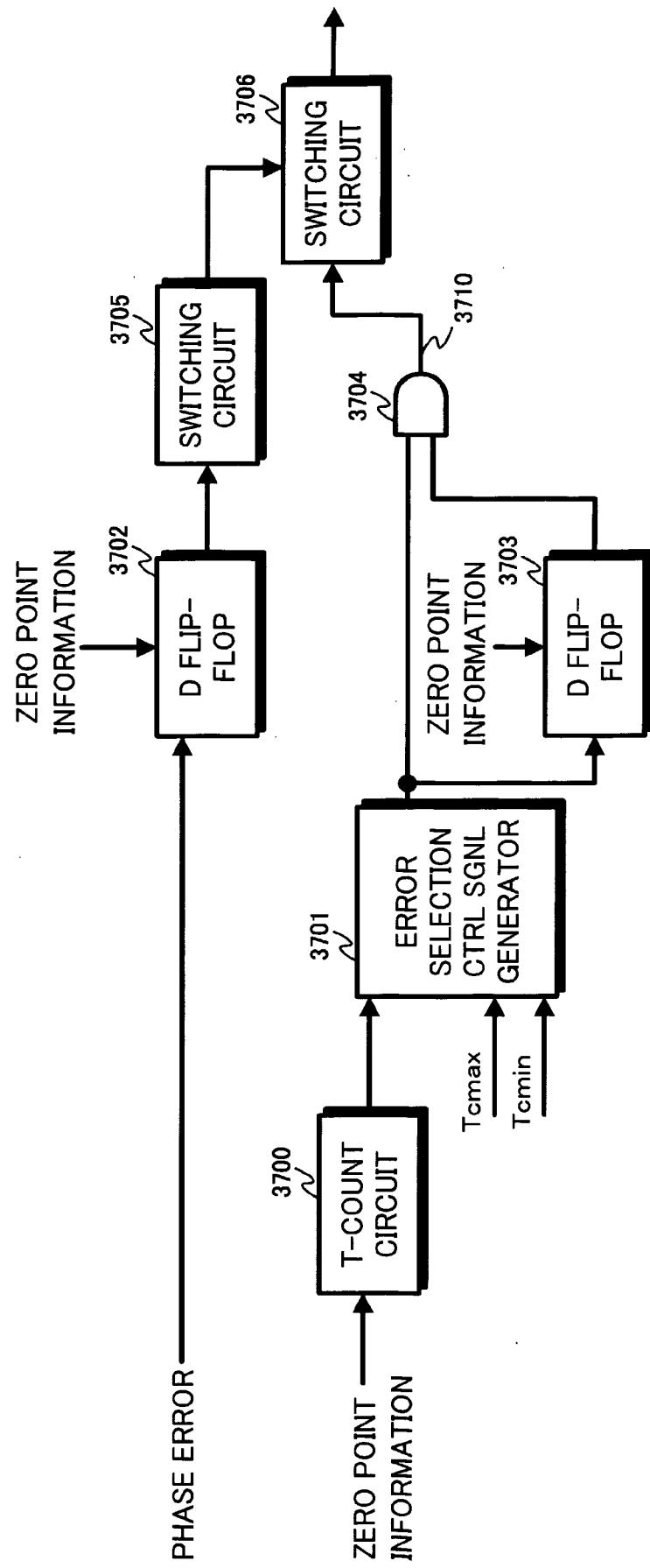


FIG.38

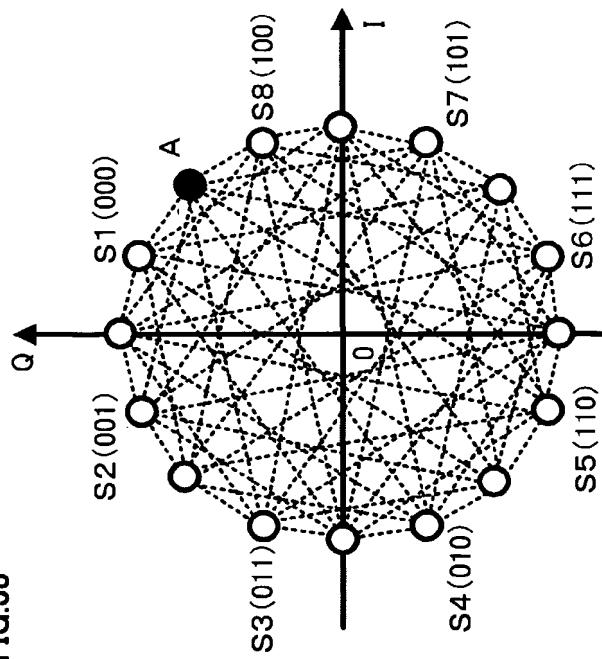


FIG.39

	BIT X_n	X_{n+1}	X_{n+2}	PHASE TRANSITION
S1	0 0 0			$\pi/8$
S2	0 0 1			$3\pi/8$
S3	0 1 1			$5\pi/8$
S4	0 1 0			$7\pi/8$
S5	1 1 0			$-7\pi/8$
S6	1 1 1			$-5\pi/8$
S7	1 0 1			$-3\pi/8$
S8	1 0 0			$-\pi/8$

FIG.40

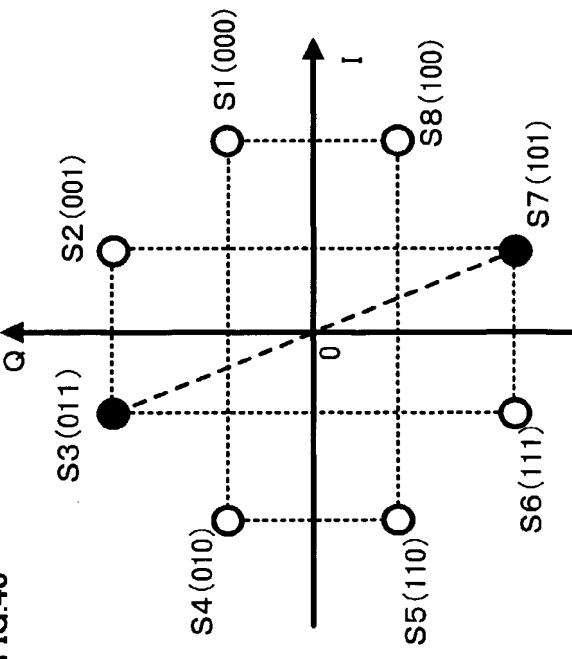


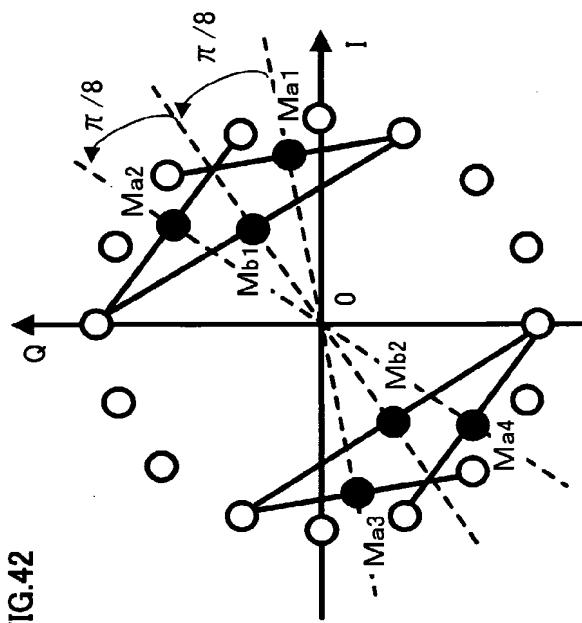
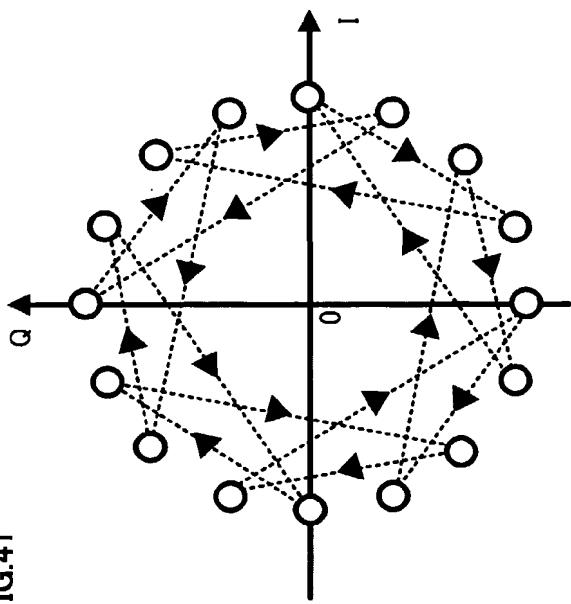
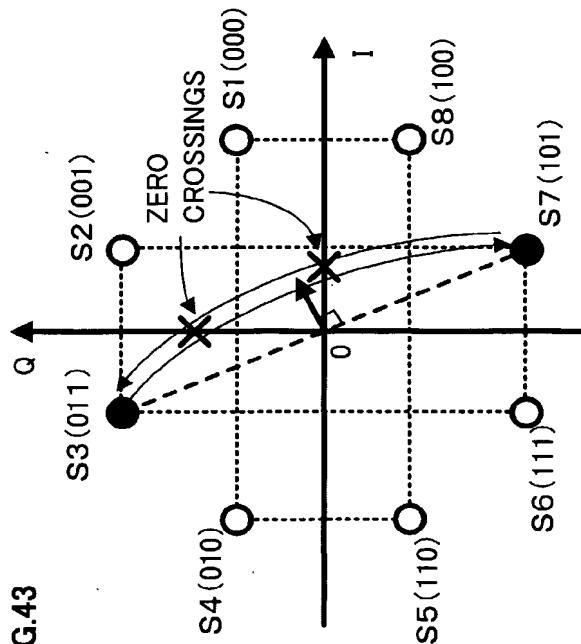
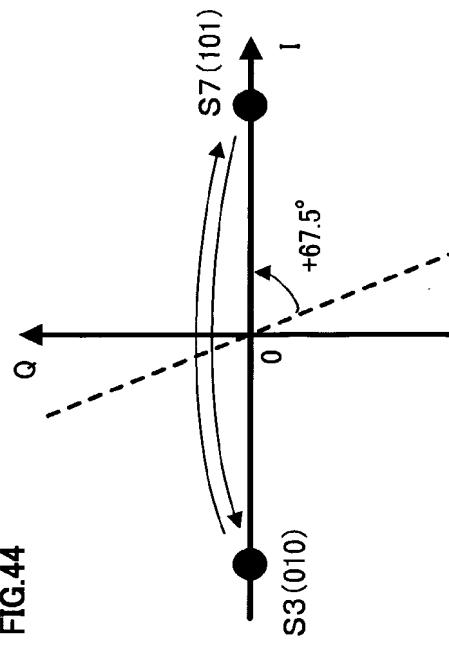
FIG.41**FIG.43****FIG.44**

FIG.45

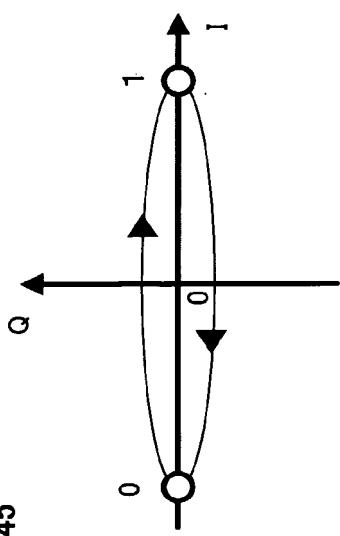


FIG.45

BIT X_n	PHASE TRANSITION	
	0	π
0	0	
1		π

FIG.46

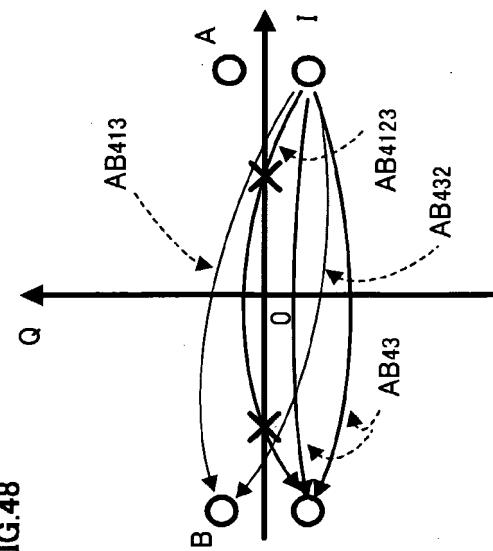


FIG.48

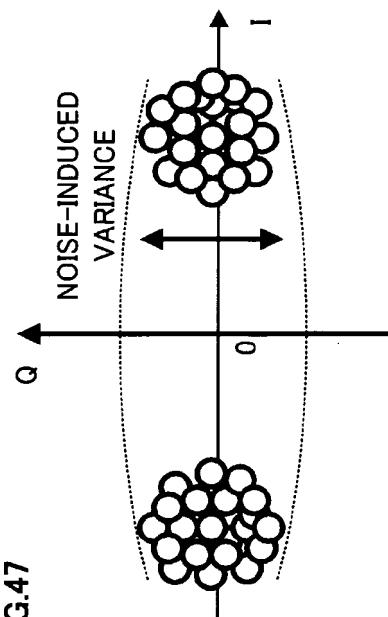


FIG.47

FIG.49

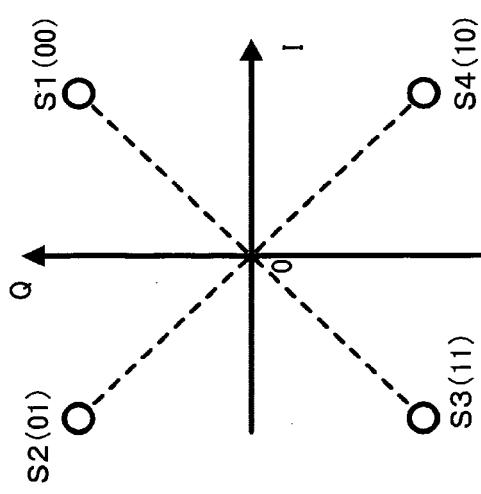


FIG.50

	BIT X_n	X_{n+1}	PHASE TRANSITION
S1	0	0	$\pi/4$
S2	0	1	$3\pi/4$
S3	1	1	$-3\pi/4$
S4	1	0	$-\pi/4$

FIG.51

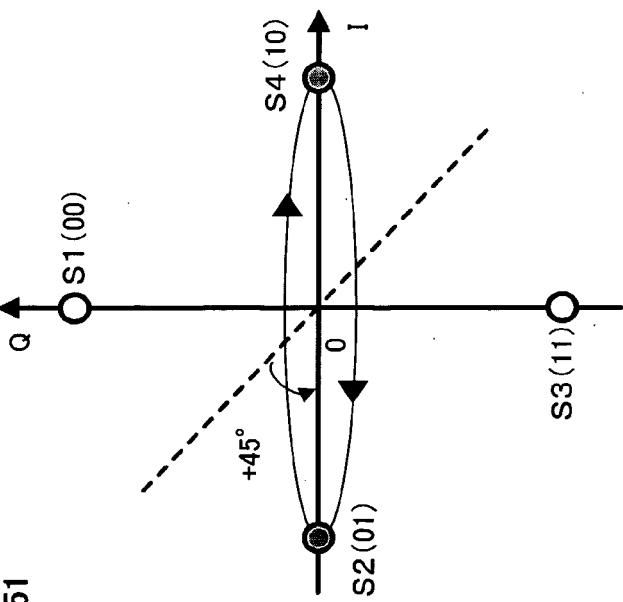


FIG.52

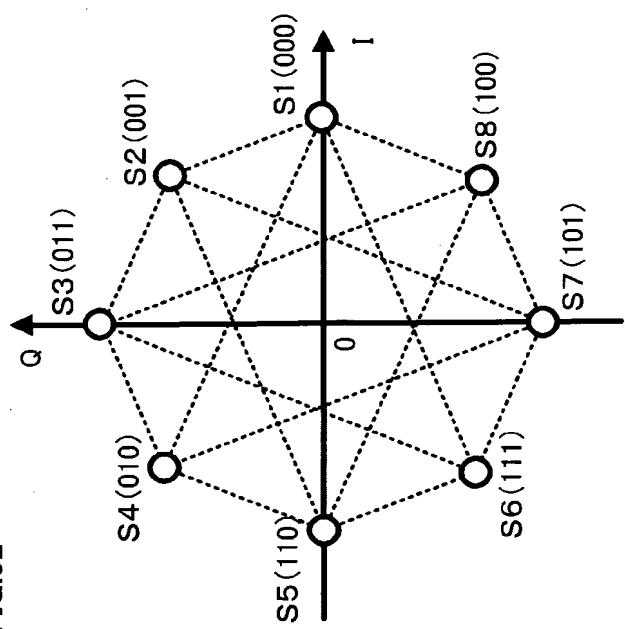


FIG.53

	BIT X _n	X _{n+1}	X _{n+2}	PHASE TRANSITION
S ₁	0	0	0	0
S ₂	0	0	1	$\pi/4$
S ₃	0	1	1	$2\pi/4$
S ₄	0	1	0	$3\pi/4$
S ₅	1	1	0	π
S ₆	1	1	1	$-3\pi/4$
S ₇	1	0	1	$-2\pi/4$
S ₈	1	0	0	$-\pi/4$

FIG.54

